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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,601	11/07/2001	Dongyun Lee	59472-8821US	8571

25096 7590 01/12/2007

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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/045,601	LEE ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on October 5, 2006, PROSECUTION IS HEREBY REOPENED. Anew ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

1-8-07

Response to Amendment

2. This Office Action is in response to the Appeal Brief filed on October 5, 2006 in response to PTO Office Action mailed on September 12, 2005. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. Claims 1-22 are pending.

Response to Arguments

4. Applicant's arguments, see Appeal brief, filed October 5, 2006, with respect to the rejection(s) of claim(s) 1-22 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Miller (5,987,577).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung (6,415,353) in view of Amitai (4,797,850).

As per claim 1, Leung discloses a memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising: a plurality of sections [row o section o of bank O, row I section 2 of bank 0 each stores 256-bit in the form of 8 32obit words; col. 8, lines 18-44], each section having a row enable line for each row of the memory and a column enable line for each column of the memory for enabling access to a subdivision of a word of memory [row address decoder activates the word line designated by output of row address multiplexer; column address decoder enables column address received from column address multiplexer; col. 27, lines 38-51], each section having a section enable line for enabling access to that section [identified row bank and section is accessed by cache tag memory; col. 9, lines 30-38]; for each row of each section, row enabler logic that enables the row enable line for that row of that section only when the section enable line for that section is enabled [row address decoder activates word line designated in the designated row; col. 32, lines 28-32]; and for each section, column enabler logic that enables a column enable line for that section only when the section enable line for that section is enabled [activation of CAS enables column address decoder which selects word in designated column address; col. 38, lines 34-37].

However, Leung does not specifically teach each section of the bank representing a subdivision of a word of memory as recited in the claim.

Amitai discloses a data processing system wherein each CAS output signal is selectively connected to an 8-bit section or byte of a data word of 16 or 32 bits to

individually access each byte in order to provide independent control of the data (col. 3, lines 18-21; col. 2, lines 11-13). Since the technology for implementing each section of a bank representing a subdivision of a word of memory was well known as evidenced by Amitai and since each section of the bank representing a subdivision of a word of memory provides independent control of the data, an artisan would have been motivated to implement the above memory sections in the system of Leung. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung to include each section of a bank representing a subdivision of a word of memory because it was well known to provide independent control of the data as taught by Amitai.

As per claim 2, Leung discloses the memory bank is part of a multi-port memory device and wherein the section enable lines are enabled based on the accessing port [data is retired through a first port and written through a second port; col. 21, lines 3-10].

As per claim 3, Leung discloses different rows of different sections can be simultaneously accessed to satisfy different memory access requests [banks can operate independent of each other so that parallel operations can take lace simultaneously; col. 6, lines 45-48].

As per claim 4, Leung discloses the row and column address enable signals are buffered to accommodate row and column latencies [row and columns addresses are buffered; col. 14, lines 8-10; col. 30, lines 23-34].

As per claim 5, Leung discloses the memory bank includes configuration information storage for selectively enabling sections [row and sections of DRAM are selected for writing to cache; col. 8, lines 15-37].

7. Claims 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung (6,415,353) in view of Amitai (4,797,850) and further in view of Miller (5,987,577).

As per claim 7, Leung discloses a memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections [row o section o of bank 0, row 1 section 2 of bank 0 each stores 256-bit in the form of 8 32-bit words; col. 8, lines 18-44], each word of memory being accessible via an address [activation of CAS enables column address decoder which selects word in designated column address; col. 38, lines 34-37], each section being selectively enabled so that row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed wherein only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled [identified row bank and

section is accessed by cache tag memory; col. 9, lines 30-38; row address decoder activates word line designated in the designated row; col. 32, lines 28-32; enabled sections inherently use more power than sections that are not enabled; col. 38, lines 34-37].

However, Leung does not specifically teach each section of the bank representing a subdivision of a word of memory as recited in the claim.

Amitai discloses a data processing system wherein each CAS output signal is selectively connected to an 8-bit section or byte of a data word of 16 or 32 bits to individually access each byte in order to provide independent control of the data (col. 3, lines 18-21; col. 2, lines 11-13). Since the technology for implementing each section of a bank representing a subdivision of a word of memory was well known as evidenced by Amitai and since each section of the bank representing a subdivision of a word of memory provides independent control of the data, an artisan would have been motivated to implement the above memory sections in the system of Leung. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung to include each section of a bank representing a subdivision of a word of memory because it was well known to provide independent control of the data as taught by Amitai.

Though Amitai discloses enabling and disabling access to a section of a memory bank representing a subdivision of a word of memory [col. 3, ll 18-21], Miller also discloses preserving power by not enabling a section of a memory bank representing a subdivision of a word of memory, and disabling row enable lines to a section of a memory Bank representing a subdivision of a word of memory [col. 5, ll 10-30] to lower the power consumption in the event a full array access does not occur [col. 10, ll 38-42].

Since the technology for implementing a memory bank having words with preserving power by not enabling a section of a memory bank representing a subdivision of a word of memory, and disabling row enable lines to a section of a memory Bank representing a subdivision of a word of memory was well known as evidenced by Miller, an artisan would have been motivated to implement this feature in the system of Leung and Amitai in order to lower the power consumption in the event a full array access does not occur. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant, to modify the system of Leung and Amitai to include preserving power by not enabling a section of a memory bank representing a subdivision of a word of memory, and disabling row enable lines to a section of a memory Bank representing a subdivision of a word of memory since this would have lowered the power consumption in the event a full array access does not occur [col. 10, ll 38-42] as taught by Miller.

As per claim 8, Leung discloses the address is divided into a row portion and a column portion and the memory bank includes a row decoder and a column decoder to

selectively accesses a word of the memory bank [RAS"# and CAS# are issued to bank 0 and decoded by decoders 182 and 183; Fig. 1; col. 11, line 64- col. 12, line 38].

As per claim 9, Leung discloses output of the row decoder and output of the column decoder only drives sections that are enabled [row address decoder activates the word line designated by output of row address multiplexer; column address decoder enables column address received from column address multiplexer; col. 27, lines 38-51].

As per claim 10, Leung discloses the outputs are buffered to accommodate row and column latencies [row and columns addresses are buffered; col. 14, lines 8-10; col. 30, lines 23-34].

As per claim 11, Leung discloses the memory bank is part of a multi-port memory device and wherein the section enable lines are enabled based on the accessing port [data is retired through a first port and written through a second port; col. 5, lines 15-20].

As per claim 12, Leung discloses different rows of different sections can be simultaneously accessed to satisfy different memory access requests [banks can operate independent of each other so that parallel operations can take lace simultaneously; col. 6, lines 45-48].

As per claim 13, Leung discloses the memory bank includes configuration information storage for selectively enabling sections [row and sections of DRAM are selected for writing to cache; col. 8, lines 15-37].

8. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung (US6,415,353) and Amitai (US4,797,850), Miller (5,987,577) and Getzinger et al. (US4,972,314).

As per claims 6 and 14, the combination of Leung and Amitai discloses the claimed invention as detailed above in the previous paragraphs. However, Leung, Amitai, and Miller do not specifically teach disabling the sections on a port-by-pod basis as recited in the claims.

Getzinger discloses a memory storage element divided into sections of equal size wherein each section has a multiplexed input/output port that provides one of four data paths in order to provide a partitioned memory for elimination of memory access contention (col. 1, lines 40-42; col. 32, lines 33-47).

Since the technology for implementing disabling the sections on a port-by-pod basis was well known as evidenced by Getzinger and since a partitioned memory for elimination of memory access contention, an artisan would have been motivated to implement disabling the sections on a pod-by-port basis in the system of Leung,

Amitai, and Miller. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung, Amitai and Miller to include disabling the sections on a pod-by-port basis because it was well known to provide a partitioned memory for elimination of memory access contention as taught by Getzinger.

9. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amitai (US4,797,850), Leung (US6,415,353), and further in view of Miller (5,987,577).

As per claims 15 and 20, the rationale in the rejection of claim 7 is herein incorporated. Amitai further discloses a method for providing access to a memory, the method comprising: disabling a section of memory [output signals are selectively connected to a different section, thus sections can be enabled or disabled selectively; col. 3, lines 18-21], the memory including multiple sections that each contain a subdivision of a word [each section contains 8-bitofa 16-bitor32-bitdata word; col. 3, lines 18-21]; receiving an address for a word of memory to be accessed [controller provides address to array of memory banks; col. 3, lines 12-17]; and accessing a subdivision of the addressed word of memory, the accessed subdivision not including the subdivision of the word in the disabled section of memory so that power is preserved by disabling the section of memory when access to the entire word is not needed [a different 8-bit section is selectively and individually accessed, thus the non-

accessed section would be disabled; inherently, a non-accessed or disables section only consumes a small amount of power as opposed to an enabled section as is inherent in the art; col. 3, lines 18-21].

However, Amitai does not specifically teach row enable lines to the disabled section are not enabled when a word of memory is accessed as recited in the claims.

Leung discloses a system wherein identified row bank and section is accessed by cache tag memory (col. 9, lines 30-38) and row address decoder activates word line designated in the designated row (col. 32, lines 28-32) to provide a plurality of independently controlled memory banks (col. 3, lines 3-4). Since the technology for implementing a system wherein row enable lines to the disabled section are not enabled when a word of memory is accessed was well known as evidenced by Leung, an artisan would have been motivated to implement this feature in the system of Amitai and Miller.

Thus, it would have been obvious to one of ordinary skill in the art, at the time of the invention to modify the system of Amitai and Miller to include row enable lines to the disabled section are not enabled when a word of memory is accessed because it was well known to provide a plurality of independently controlled memory banks (col. 3, lines 3-4).

10. Claims 16-19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amitai (US 4,797,850) and Leung (US 6,415,353), Miller (5,987,577) and Getzinger et al. (US 4,972,314).

As per claims 16 and 21, the combination of Amitai, Leung, and Miller discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Amitai, Leung, and Miller does not specifically teach disabling the sections on a port-by-port basis as recited in the claims.

Getzinger discloses a memory storage element divided into sections of equal size wherein each section has a multiplexed input/output port that provides one of four data paths in order to provide a partitioned memory for elimination of memory access contention (col. 1, lines 40-42; col. 32, lines 33-47).

Since the technology for implementing disabling the sections on a port-by-port basis was well known as evidenced by Getzinger and since a partitioned memory for elimination of memory access contention, an artisan would have been motivated to implement disabling the sections on a port-by-port basis in the system of Amitai, Leung, and Miller. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Amitai, Leung, and MIller to include disabling the sections on a port-by-port basis because it was well known to provide a partitioned memory for elimination of memory access contention as taught by Getzinger.

As per claim 17, Getzinger discloses different subdivisions of a word can be accessed through different ports [each section has one port and the memory controller determines which ports active; col. 32, lines 33-56].

As per claims 18, 19 and 22, Amitai discloses a latch storing information about enabling or disabling a section [col. 5, lines 2-12].

Conclusion

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung can be reached on **(571) 272-6799**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 5, 2007

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
1-8-07

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Examiner
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